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Introduction

Filters are used in a variety of applications, and throughout many different industries. The requirements are determined by both, application and the industry that is using the part.

For instance, in automotive applications, parts within the vehicle are subjected to varying temperatures all day long, whether the vehicle is cruising on a mountain highway in Colorado or strolling up and down the Vegas strip in 110°F temperatures.

Many parts are also subjected to extreme heat in the engine compartment of the automobile as well. For this reason, Automotive OEM’s are very strict on qualify parts and obtaining the worst-case analysis on parts for these scenarios.

For these applications, temperature changes are clearly a factor on the design. Resistors are highly susceptible to temperature changes. The Switched Capacitor circuit takes all of the resistors that were in the circuit, and replaces them with a capacitor and switch combination.
**Elliptic Filter Background**

Elliptic (Cauer) filters have a much narrower transition from the pass to stop band, or vice versa. The price to pay for this feature is that Elliptic filters have equal ripple in both the pass-band and the stop-band, due to the fact that they have both poles and zeroes. The zeroes are imaginary.

Another benefit of choosing an Elliptic Filter design is that the order is typically 0.25 to 0.5 less than that of the order determined through a Chebychev or Butterworth design.

While designing Chebychev filters, one must use tables to determine the normalized frequencies and quality factors. With Elliptic design, one must use a type of mathematical calculation to determine the normalized frequencies and quality factors. For this reason, Elliptic isn’t a favorite approach for Engineers to use.

It is important to note that it is becoming a must. As tolerances get smaller and smaller, the need to have a fast switching (pass-band to stop-band transition) filter is becoming greater and greater. There are also many routines that are becoming available to evaluate and design Elliptic filters to meet ones needs.
Switched Capacitor Background

Resistors tend to be very heat-sensitive, meaning the resistivity changes over temperature. Although, capacitors’ characteristics change slightly over temperature as well, they do not change nearly as much as that of a resistor.

Also, resistors are almost impossible to implement within IC’s, while maintaining a small size. Capacitors and switches have been implemented on IC’s for over 20 years now. It is incredible how small the IC’s have become over the year.

Based on the requirements of a small chip size, and a low tolerance to heat, Switched Capacitor filters are in high demand. Automotive suppliers all over the world almost exclusively use Switch Capacitor filters.

More and more electronics are added to an automobile every year. And besides the SUV growth in popularity, it seems vehicles are continuing to become smaller and smaller. With more components, and less space, board size requirements are becoming ridiculously small. Instead of having a board population of 15 resistor/capacitor/op-amp combinations, all that is needed is one small IC, with a couple of resistors determining the mode of operation.
GIC Circuit

The GIC circuit is used to implement a high-pass, low-pass, band-pass, all-pass, notch, high-pass notch, and low-pass notch. The variables are determined, and will determine the component values. An example of how these variables effect the transfer function is shown in Figure 1.

Generic Transfer Function

\[
H_s \equiv \frac{\alpha s^2 + \beta \left( \frac{\omega_0}{Q} \right) + c \cdot \omega_0^2}{s^2 + \frac{\omega_0}{Q}(s) + \omega_0^2}
\]

\[
\begin{align*}
\alpha &:= 2a - c \\
\beta &:= 2b - c \\
c &:= 2b
\end{align*}
\]

Figure 1: GIC Circuit
Design Process

The specifications were first inputted into Matlab. They consisted of the attenuation requirements and the cutoff frequency requirements.

Matlab determined the normalized frequencies, and gave us the normalized transfer function of the circuit.

MathCad was used to denormalize the circuit. It also determined our quality factors. Once denormalized, the designed parameters could be obtained. Since a GIC circuit was used, calculating the factors a, b, and c was necessary. Once these values were obtained, the component values were calculated.

PSPICE was used to simulate our design. We were able to see the magnitude and phase response, and verify that the filter was designed correctly. We were also able to put standard values in place of the “designed” values to determine what effect that had on our circuit operation.
Filter Design Specifications

Low Pass Notch Filter

Specification
Our specifications for the Low Pass Notch filter consisted of a pass-band frequency of 200Hz. The stop-band frequency was chosen to be 225Hz. The attenuation in the pass-band cannot fall beneath 2dB. The attenuation in the stop-band cannot rise about 17dB.

High Pass Notch Filter

Specification
Our specifications for the Low Pass Notch filter consisted of a pass-band frequency of 200Hz. The stop-band frequency was chosen to be 225Hz. The attenuation in the pass-band cannot fall beneath 2dB. The attenuation in the stop-band cannot rise about 17dB.

Band Pass Filter

Specification
Our specifications for the Low Pass Notch filter consisted of a pass-band frequency of 200Hz through 7kHz. The stop-band frequency was chosen to be 225Hz and 7.5kHz. The attenuation in the pass-band cannot fall beneath 2dB. The attenuation in the stop-band cannot rise about 17dB.
PSPICE Simulations

**Low Pass Notch Filter**

The low pass filter magnitude response is shown in **Figure 2**. As shown in the plot, the actual simulated value of the cutoff frequency is within 0.1% of the specified value. Figure 3 shows the magnitude response using standard values for the components. Also noted is that the cutoff frequency is within 0.1% for this design as well. **Figure 4** and **Figure 5** show the phase responses for both cases.

**Magnitude Response**

![Magnitude Response Graph](graph.png)

**Figure 2:** Magnitude Response of LP Notch Filter using ideal values
Figure 3: Magnitude Response of LP Notch Filter using standard values
Phase Response

Figure 4: Phase Response of LP Notch Filter using ideal values

Figure 5: Phase Response of LP Notch Filter using standard values
**High Pass Notch Filter**

Figure 6 and Figure 7 show the magnitude response of the HP Notch filters. As with the LP notch design, the values of the cutoff frequencies are very close to the specified design, although not as close as in the case of the LP Notch design. The phase responses are shown in Figure 8 and Figure 9.

**Magnitude Response**

![Magnitude Response of HP Notch Filter using ideal values](image)

Figure 6: Magnitude Response of HP Notch Filter using ideal values
Figure 7: Magnitude Response of HP Notch Filter using ideal values

Phase Response

Figure 8: Phase Response of HP Notch Filter using ideal values
Figure 9: Phase Response of HP Notch Filter using standard values
**Band-Pass Notch Filter**

Figure 10 and Figure 11 show the magnitude response of the BP Notch filters. As with the LP & HP notch design, the values of the cutoff frequencies are very close to the specified design, although not as close as in the case of the LP Notch design. The phase responses are shown in Figure 12 and Figure 13.

**Magnitude Response**

![Magnitude Response of Band-Pass Filter using ideal values](image)

*Figure 10: Magnitude Response of Band-Pass Filter using ideal values*
Figure 11: Magnitude Response of Band-Pass Filter using ideal values
Phase Response

Figure 12: Phase Response of Band-Pass Filter using ideal values

Figure 13: Phase Response of Band-Pass Filter using standard values
Hardware Design

**MF10 Operation**

The switched capacitor IC chip that was used is the MF10 by National Semiconductor. The MF10 is a universal monolithic dual switched capacitor filter. It has two independent, 2nd order CMOS active filter building blocks. With the use of an external clock and three to four external resistors, this IC can be configured to perform a Low-Pass, High-Pass, Band-Pass, notch, or allpass filter. A 4th order filter can be obtained by cascading two of the 2nd order filter building blocks. A Butterworth, Chebyshev, Elliptic, and a Bessel-Thomson filter configuration can be achieved with this IC.

There are six different modes of operation from this IC that can realize the different types of filters. For example, the High-Pass filter can be realized only from modes 3, 3a, and 6a. In the MF10 datasheet, these modes are described along with needed equations to calculate the external resistor values. There are also schematics that are provided for each of the modes to show the user how to wire the IC.
For the Low-Pass filter that was built, this the equation section for Mode 2 which was used in Figure 14:

Figure 14: Equations used to design MF10 Implementation for the LP Notch Filter
This is the schematic that is provided by National Instruments for the Low-Pass filter, Mode 2 in Figure 15:

Figure 15: Internal Schematic of the MF10 IC for the Low Pass Notch Filter
For the High-Pass and the Band-Pass filters, Mode 3 was chosen. Here are the equations for Mode 3 in Figure 16:

**MODE 3: Highpass, Bandpass, Lowpass Outputs**
*(See Figure 10)*

\[
\begin{align*}
    f_O &= \frac{f_{\text{CLK}}}{100} \times \sqrt{\frac{R_2}{R_4}} \quad \text{or} \quad f_{\text{CLK}} \times \frac{\sqrt{R_2}}{50} \times \sqrt{\frac{R_2}{R_4}} \\
    Q &= \text{quality factor of the complex pole pair} \\
    &= \frac{\sqrt{R_2}}{\sqrt{R_4}} \times \frac{R_3}{R_2} \\
    H_{\text{OHp}} &= \text{Highpass Gain} \left( \text{as } f \rightarrow \frac{f_{\text{CLK}}}{2} \right) = -\frac{R_2}{R_1} \\
    H_{\text{OBP}} &= \text{Lowpass Gain} \left( \text{at } f = f_O \right) = -\frac{R_3}{R_1} \\
    H_{\text{OLP}} &= \text{Lowpass Gain} \left( \text{as } f \rightarrow 0 \right) = -\frac{R_4}{R_1} \\
    \text{Circuit dynamics:} \quad \frac{R_2}{R_4} = \frac{H_{\text{OHp}}}{H_{\text{OLP}}} \\
    H_{\text{OBP}} &= \sqrt{H_{\text{OHp}} \times H_{\text{OLP}}} \times Q \\
    H_{\text{OLP}(\text{peak})} &\approx Q \times H_{\text{OLP}} \text{ (for high } Q'\text{'s)} \\
    H_{\text{OHp}(\text{peak})} &\approx Q \times H_{\text{OHp}} \text{ (for high } Q'\text{'s)}
\end{align*}
\]

Figure 16: Equations used to design MF10 Implementation for the HP Notch Filter and Band-Pass Filter
This is the schematic that is provided by National Instruments for the high-pass and band-pass filters, Mode 3 in Figure 17:

![Schematic of the MF10 IC for the High-Pass Notch and Band-Pass Filters](image)

**Figure 17: Internal Schematic of the MF10 IC for the High-Pass Notch and Band-Pass Filters**

The IC can be configured to operate on a single power supply (+10V) or a dual supply (+/- 5V). The +/- 5V-supply configuration was used. The datasheet also provides some examples for a Low-Pass filter. This example was followed for the lowapss filter that was built and was successful. The High-Pass and the Band-Pass filters were also modeled after the example, however, neither of these filters was realizable.

The calculations of how the MF10 parts were configured for each type of filter can be found in the appendix, while the actual schematics for each design are shown in **Figure 18, Figure 19, and Figure 20**.
Figure 18: Schematic using the MF10 IC for the Low-Pass Notch design
Figure 19: Schematic using the MF10 IC for the High-Pass Notch design
BPF

NOTES: MODE 3
wc = 1.323kHz
CLK = 66.14kHz

Figure 20: Schematic using the MF10 IC for the Band-Pass design
Conclusion

The design of Elliptic and/or Switched Capacitor filters is pretty straightforward, however much more tedious than that of a Chebychev or Butterworth design. There were also more considerations that had to take place, and the biggest being how to find an IC to implement this with.

Once the chip was found, the MF10 by National Semiconductor, determining how the Switched Capacitor chip should be wired up is the hardest portion of the whole design. The Low-Pass design was very successful as shown in the plots in Figure 21, Figure 22, Figure 23, and Figure 24. In these plots, the input frequency is shown in yellow, while the output frequency is shown in pink. It is shown that as the frequency increases, the output amplitude decreases, as designed. For example, noted in Figure 23 (400 Hz), the amplitude is small, but the output frequency is somewhat noticeable. In Figure 24 (1 kHz) it is unrecognizable.
Figure 21: Low-Pass Notch Realization passing the frequency of 100Hz
Figure 22: Low-Pass Notch Realization passing the frequency of 200Hz
Figure 23: Low-Pass Notch Realization stopping the frequency of 400 Hz
Finally, the actual design of our part is shown in Figure 25 and Figure 26. As seen, it is a somewhat complex design. The design was such that the High-Pass and Band-Pass sections were laid out the same so that debugging any potential problems in the circuit would be universal for the 3 filters.
Figure 25: Overview of the final implementation of all 3 circuits on a breadboard
Figure 26: Up close view of the final implementation of all 3 circuits on a breadboard
Appendix I: Matlab Code

a) Low-Pass Design

% Filter specifications
fp = 200; % Pass band frequency edge
ap = 2; % Pass band attenuation
fs = 225; % Stop band frequency edge
as = 17; % Stop band attenuation
% Frequency Normalization
kf = 2*pi*fp % Frequency scaling Factor
wp = 1 % Normalized pass band frequency in Rad / Sec
ws = 2*pi*fs/kf % Stop band normalized frequency
% Find the order of the elliptic filter
[n,wn] = ellipord (wp,ws,ap,as,'s')
% Finding the transfer function
% Numerator and Denominator coefficients
[num,den] = ellip (n,ap,as,wn,'s')
% Plotting the frequency response
w = [0:.01:4]; % Frequency Vector Rad / Sec
H = Freqs (num,den,w); % Frequency Response
magdb = 20*log10(abs(H)); % Magnitude Response in dB
plot(w,magdb)
xlabel('Freq. in rad./sec.')
ylabel('Mag.,dB')
grid on
plot(w,-magdb); % Attenuation
xlabel('Freq. in rad./sec.')
ylabel('Att.,dB')
grid on;
% Factoring the transfer function
% First and second order section
[sos,g]=tf2sos(num,den)
b) High-Pass Design

%Elliptic HP Filter Design

%Attenuation Requirements

as=20
ap=0.5

wp=2*pi*7e3
ws=2*pi*6e3
kf=wp/1
wpn=wp/kf
wsn=ws/kf

%Finding the Order
[n,wn]=ellipord(wpn, wsn,ap,as,'s');
fprintf('
 The order of the required filter is: %f',n)

%Finding the Transfer Function of normalized case
[num,den]=ellip(n,ap,as,wn,'high','s');

%Plot the Frequency Response

w=[0:.01:3];
H=freqs(num,den,w);
magdB=20*log10(abs(H));
plot(kf*w/(2*pi),magdB)
xlabel('Frequency (Hz)')
ylabel('Magnitude Response (dB)')
grid on

plot(kf*w/(2*pi), -magdB)
xlabel('Frequency (Hz)')
ylabel('Attenuation (dB)')
title('Attenuation Characteristics of Elliptic Filter')
grid on

%Factoring the Transfer Function

[sos,g]=tf2sos(num,den);
sos
g
c) Band-Pass Design

% Elliptic BPF Specs
fsl=200;    %Lower stopband in Hz
wsl=2*pi*fsl;
fpl=250;   %Lower passband in Hz
wpl=2*pi*fpl;
fpu=7000;   %Upper passband in Hz
wpu=2*pi*fpu;
fsu=7500;   %Upper stopband in Hz
wsu=2*pi*fsu;
ap=5;     %Alpha pass
as=10;      %Alpha stop

% Frequency Normalization
f0=sqrt(fpl*fpu);
w0=2*pi*f0;
kf=w0;
wpn=[wpl wpu]/kf;
wsn=[wsl wsu]/kf;

% Finding order & transfer function (norm)
[n,wn]=ellipord(wpn,wsn,ap,as,'s');
[num,den]=ellip(n,ap,as,wn,'s');
fprintf('
The order of the Elliptic BPF is: %f',n*2)
fprintf('')

%Plotting the Responses & Attenuation
w=[0:0.01:7]';  %Setting a freq scale
H=freqs(num,den,w);
magdB=20*log10(abs(H));
subplot(2,1,1)
plot(kf*w/(2*pi),magdB);   %Plotting mag resp
grid on;
xlabel('Frequency, Hz');
ylabel('Magnitude, dB');
title('Magnitude Response');
subplot(2,1,2)
plot(angle(H));   %Plotting phase resp
grid on;
xlabel('Frequency, Hz');
ylabel('Phase, rad');
title('Phase Response');
figure
plot(kf*w/(2*pi),-magdB);  %Plotting atten
grid on;
xlabel('Frequency, Hz');
ylabel('Attenuation, dB');
title('Attenuation');
figure
freqs(num,den)  %Plotting freq resp
tf(num,den)     %Finding the transfer function
[sos,g]=tf2sos(num,den) %Factoring of the trans func
Appendix II: Calculations for the PSPICE Design

a) Low-Pass Notch Design

From Matlab,

\[ n := 4 \]

Calculations of Normalized Frequencies and Quality Factors

<table>
<thead>
<tr>
<th>1st Stage</th>
<th>2nd Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \omega_{z1} := \sqrt{2.9183} )</td>
<td>( \omega_{z2} := \sqrt{1.1082} )</td>
</tr>
<tr>
<td>( \omega_{z1} = 1.708 )</td>
<td>( \omega_{z2} = 1.053 )</td>
</tr>
<tr>
<td>( \omega_{01} := \sqrt{0.9922} )</td>
<td>( \omega_{02} := \sqrt{0.5799} )</td>
</tr>
<tr>
<td>( \omega_{01} = 0.996 )</td>
<td>( \omega_{02} = 0.762 )</td>
</tr>
<tr>
<td>( Q1 := \frac{\omega_{01}}{0.0492} )</td>
<td>( Q2 := \frac{\omega_{02}}{0.6109} )</td>
</tr>
<tr>
<td>( Q1 = 20.246 )</td>
<td>( Q2 = 1.247 )</td>
</tr>
</tbody>
</table>

Denormalization

\( k_f := 200 \cdot 2 \cdot \pi \)
\( k_f = 1.257 \times 10^3 \)

\( \omega _{z1\text{Den}} := k_f \omega _{z1} \)
\( \omega _{z1\text{Den}} = 2.147 \times 10^3 \)

\( \omega _{z2\text{Den}} := k_f \omega _{z2} \)
\( \omega _{z2\text{Den}} = 1.323 \times 10^3 \)

\( \omega _{01\text{Den}} := k_f \omega _{01} \)
\( \omega _{01\text{Den}} = 1.252 \times 10^3 \)

\( \omega _{02\text{Den}} := k_f \omega _{02} \)
\( \omega _{02\text{Den}} = 956.944 \)
Finding the DC Gain

\[ H_{j0} := 0.794 \]

\[ H_{1j0} := \sqrt{H_{j0}} \]
\[ H_{1j0} = 0.891 \]
\[ H_{2j0} := \sqrt{H_{j0}} \]
\[ H_{2j0} = 0.891 \]

\[ g_1 := \frac{\omega_{01} \cdot H_{1j0}}{2} \cdot H_{j0} \]
\[ g_1 = 0.303 \]
\[ g_2 := \frac{\omega_{02} \cdot H_{2j0}}{2} \cdot H_{j0} \]
\[ g_2 = 0.466 \]

Finding a, b, and c from GIC Circuit

\[ c_1 := \frac{g_1 \cdot \omega_{z1}}{2} \cdot \omega_{01} \]
\[ c_1 = 0.891 \]
\[ c_2 := \frac{g_2 \cdot \omega_{z2}}{2} \cdot \omega_{02} \]
\[ c_2 = 0.891 \]

\[ b_1 := \frac{c_1}{2} \]
\[ b_1 = 0.446 \]
\[ b_2 := \frac{c_2}{2} \]
\[ b_2 = 0.446 \]

\[ a_1 := \frac{(g_1 + c_1)}{2} \]
\[ a_1 = 0.597 \]
\[ a_2 := \frac{(g_2 + c_2)}{2} \]
\[ a_2 = 0.679 \]

Generic Transfer Function

\[ H_s \equiv \frac{\alpha \cdot s^2 + \frac{\beta}{\alpha} \left( \frac{\omega_0}{Q} \right) + c \cdot \frac{\omega_0^2}{\alpha}}{s^2 + \frac{\omega_0}{Q} (s) + \omega_0^2} \]
\[ \alpha := 2a - c \]
\[ \beta := 2b - c \]
\[ c := 2b \]
Setting Up Component Values

\[ \text{Cap} := 10 \cdot 10^{-9} \]

\[ R_{1st1} := \frac{1}{\text{Cap} \cdot \omega_{01}\text{Den}} \]

\[ R_{1st1} = 7.989 \times 10^4 \]

\[ R_{1st2} := Q_1 \cdot \frac{R_{1st1}}{b_1} \]

\[ R_{1st2} = 3.63 \times 10^6 \]

\[ R_{1st3} := Q_1 \cdot \frac{R_{1st1}}{1 - b_1} \]

\[ R_{1st3} = 2.917 \times 10^6 \]

\[ R_{1st4} := \frac{R_{1st1}}{c_1} \]

\[ R_{1st4} = 8.966 \times 10^4 \]

\[ R_{1st5} := \frac{R_{1st1}}{1 - c_1} \]

\[ R_{1st5} = 7.334 \times 10^5 \]

\[ C_{1st1} := a_1 \cdot \text{Cap} \]

\[ C_{1st1} = 5.97 \times 10^{-9} \]

\[ C_{1st2} := (1 - a_1) \cdot \text{Cap} \]

\[ C_{1st2} = 4.03 \times 10^{-9} \]

\[ R_{2nd1} := \frac{1}{\text{Cap} \cdot \omega_{02}\text{Den}} \]

\[ R_{2nd1} = 1.045 \times 10^5 \]

\[ R_{2nd2} := \frac{Q_2 \cdot R_{2nd1}}{b_2} \]

\[ R_{2nd2} = 2.924 \times 10^5 \]

\[ R_{2nd3} := Q_2 \cdot \frac{R_{2nd1}}{1 - b_2} \]

\[ R_{2nd3} = 2.349 \times 10^5 \]

\[ R_{2nd4} := \frac{R_{2nd1}}{c_2} \]

\[ R_{2nd4} = 1.173 \times 10^5 \]

\[ R_{2nd5} := \frac{R_{2nd1}}{1 - c_2} \]

\[ R_{2nd5} = 9.593 \times 10^5 \]

\[ C_{2nd1} := a_2 \cdot \text{Cap} \]

\[ C_{2nd1} = 6.787 \times 10^{-9} \]

\[ C_{2nd2} := (1 - a_2) \cdot \text{Cap} \]

\[ C_{2nd2} = 3.213 \times 10^{-9} \]
b) *High-Pass Notch Design*

From Matlab,

\[ n := 4 \]

**Calculations of Normalized Frequencies and Quality Factors**

<table>
<thead>
<tr>
<th>1st Stage</th>
<th>2nd Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ \omega_{z1} := \sqrt{0.2017} ]</td>
<td>[ \omega_{z2} := \sqrt{0.7251} ]</td>
</tr>
<tr>
<td>[ \omega_{z1} = 0.449 ]</td>
<td>[ \omega_{z2} = 0.852 ]</td>
</tr>
<tr>
<td>[ \omega_{01} := \sqrt{0.9532} ]</td>
<td>[ \omega_{02} := \sqrt{1.4486} ]</td>
</tr>
<tr>
<td>[ \omega_{01} = 0.976 ]</td>
<td>[ \omega_{02} = 1.204 ]</td>
</tr>
<tr>
<td>[ Q1 := \frac{\omega_{01}}{1.2993} ]</td>
<td>[ Q2 := \frac{\omega_{02}}{0.1113} ]</td>
</tr>
<tr>
<td>[ Q1 = 0.751 ]</td>
<td>[ Q2 = 10.814 ]</td>
</tr>
</tbody>
</table>

**Denormalization**

\[ k_f := 7.2 \cdot \pi \cdot 10^3 \]
\[ k_f = 4.398 \times 10^4 \]

\[ \omega_{\text{z1Den}} := k_f \omega_{\text{z1}}. \]
\[ \omega_{\text{z1Den}} = 1.975 \times 10^4 \]

\[ \omega_{\text{01Den}} := k_f \omega_{\text{01}} \]
\[ \omega_{\text{01Den}} = 4.294 \times 10^4 \]

\[ \omega_{\text{z2Den}} := k_f \omega_{\text{z2}} \]
\[ \omega_{\text{z2Den}} = 3.745 \times 10^4 \]

\[ \omega_{\text{02Den}} := k_f \omega_{\text{02}} \]
\[ \omega_{\text{02Den}} = 5.294 \times 10^4 \]
Finding the DC Gain

\[ H_{j0} = 0.1 \]

\[ H_{j0} := \sqrt{H_{j0}} \]

\[ H_{j0} = 0.316 \]

\[ H_{j0} := \sqrt{H_{j0}} \]

\[ H_{j0} = 0.316 \]

\[ g_1 := \frac{\omega_{01}^2 \cdot H_{j0}}{\omega_{z1}} \]

\[ g_1 = 1.494 \]

\[ g_2 := \frac{\omega_{02}^2 \cdot H_{j0}}{\omega_{z2}} \]

\[ g_2 = 0.632 \]

Finding a, b, and c from GIC Circuit

\[ a_1 := \frac{(g_1 + c_1)}{2} \]

\[ a_1 = 0.905 \]

\[ a_2 := \frac{(g_2 + c_2)}{2} \]

\[ a_2 = 0.474 \]

\[ a := 2a - c \]

\[ b := 2b - c \]

\[ c := 2b \]

\[ c_1 := \frac{\omega_{z1}^2}{\omega_{01}} \]

\[ c_1 = 0.316 \]

\[ c_2 := \frac{\omega_{z2}^2}{\omega_{02}} \]

\[ c_2 = 0.316 \]

\[ b_1 := \frac{c_1}{2} \]

\[ b_1 = 0.158 \]

\[ b_2 := \frac{c_2}{2} \]

\[ b_2 = 0.158 \]

Generic Transfer Function

\[ H_s = \frac{\left[ 2 + \frac{\beta}{\alpha} \left( \frac{\omega_0}{Q} \right) + c \frac{\omega_0^2}{\alpha} \right]}{s^2 + \frac{\omega_0}{Q} (s) + \omega_0^2} \]

\[ \alpha := 2a - c \]

\[ \beta := 2b - c \]

\[ c := 2b \]
Setting Up Component Values

\[ \text{Cap} := 10 \cdot 10^{-9} \]

\[ R_{1st1} := \frac{1}{\text{Cap} \cdot \omega_{01\text{Den}}} \]

\[ R_{1st1} = 2.329 \times 10^3 \]

\[ R_{1st2} := Q_1 \cdot \frac{R_{1st1}}{b_1} \]

\[ R_{1st2} = 1.107 \times 10^4 \]

\[ R_{1st3} := Q_1 \cdot \frac{R_{1st1}}{(1 - b_1)} \]

\[ R_{1st3} = 2.079 \times 10^3 \]

\[ R_{1st4} := \frac{R_{1st1}}{c_1} \]

\[ R_{1st4} = 7.364 \times 10^3 \]

\[ R_{1st5} := \frac{R_{1st1}}{(1 - c_1)} \]

\[ R_{1st5} = 3.406 \times 10^3 \]

\[ C_{1st1} := a_1 \cdot \text{Cap} \]

\[ C_{1st1} = 9.053 \times 10^{-9} \]

\[ C_{1st2} := (1 - a_1) \cdot \text{Cap} \]

\[ C_{1st2} = 9.468 \times 10^{-10} \]

\[ R_{2nd1} := \frac{1}{\text{Cap} \cdot \omega_{02\text{Den}}} \]

\[ R_{2nd1} = 1.889 \times 10^3 \]

\[ R_{2nd2} := Q_2 \cdot \frac{R_{2nd1}}{b_2} \]

\[ R_{2nd2} = 1.292 \times 10^5 \]

\[ R_{2nd3} := Q_2 \cdot \frac{R_{2nd1}}{(1 - b_2)} \]

\[ R_{2nd3} = 2.426 \times 10^4 \]

\[ R_{2nd4} := \frac{R_{2nd1}}{c_2} \]

\[ R_{2nd4} = 5.974 \times 10^3 \]

\[ R_{2nd5} := \frac{R_{2nd1}}{(1 - c_2)} \]

\[ R_{2nd5} = 2.763 \times 10^3 \]

\[ C_{2nd1} := a_2 \cdot \text{Cap} \]

\[ C_{2nd1} = 4.74 \times 10^{-9} \]

\[ C_{2nd2} := (1 - a_2) \cdot \text{Cap} \]

\[ C_{2nd2} = 5.26 \times 10^{-9} \]


c) **Band-Pass Design**

From Matlab,

\[ n := 4 \]

Calculations of Normalized Frequencies and Quality Factors

<table>
<thead>
<tr>
<th>1st Stage</th>
<th>2nd Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \omega_{z1} := \sqrt{0.0241} )</td>
<td>( \omega_{z2} := \sqrt{41.5507} )</td>
</tr>
<tr>
<td>( \omega_{z1} = 0.155 )</td>
<td>( \omega_{z2} = 6.446 )</td>
</tr>
<tr>
<td>( \omega_{01} := \sqrt{0.0414} )</td>
<td>( \omega_{02} := \sqrt{24.152} )</td>
</tr>
<tr>
<td>( \omega_{01} = 0.203 )</td>
<td>( \omega_{02} = 4.914 )</td>
</tr>
<tr>
<td>( Q_1 := \frac{\omega_{01}}{0.0515} )</td>
<td>( Q_2 := \frac{\omega_{02}}{1.2438} )</td>
</tr>
<tr>
<td>( Q_1 = 3.951 )</td>
<td>( Q_2 = 3.951 )</td>
</tr>
</tbody>
</table>

Denormalization

\( k_f := 2 \pi \sqrt{250 \cdot 7000} \)

\( k_f = 8.312 \times 10^3 \)

<table>
<thead>
<tr>
<th>1st Stage</th>
<th>2nd Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \omega_{z1Den} := k_f \omega_{z1} )</td>
<td>( \omega_{z2Den} := k_f \omega_{z2} )</td>
</tr>
<tr>
<td>( \omega_{z1Den} = 1.29 \times 10^3 )</td>
<td>( \omega_{z2Den} = 5.358 \times 10^4 )</td>
</tr>
<tr>
<td>( \omega_{01Den} := k_f \omega_{01} )</td>
<td>( \omega_{02Den} := k_f \omega_{02} )</td>
</tr>
<tr>
<td>( \omega_{01Den} = 1.691 \times 10^3 )</td>
<td>( \omega_{02Den} = 4.085 \times 10^4 )</td>
</tr>
</tbody>
</table>
Finding the DC Gain

\[ H_{j0} := 0.3162 \]

\[ H_{1j0} := \sqrt{H_{j0}} \quad H_{2j0} := \sqrt{H_{j0}} \]

\[ k_1 := \frac{\omega_{01}^2 \cdot H_{1j0}}{\omega_{z1}^2} \quad k_2 := \frac{\omega_{02}^2 \cdot H_{2j0}}{\omega_{z2}^2} \]

\[ k_1 = 0.966 \quad k_2 = 0.327 \]

Finding a, b, and c from GIC Circuit

\[ c_1 := k_1 \cdot \frac{\omega_{z1}^2}{\omega_{01}^2} \quad c_2 := k_2 \cdot \frac{\omega_{z2}^2}{\omega_{02}^2} \]

\[ c_1 = 0.562 \quad c_2 = 0.562 \]

\[ b_1 := \frac{c_1}{2} \quad b_2 := \frac{c_2}{2} \]

\[ b_1 = 0.281 \quad b_2 = 0.281 \]

\[ a_1 := \frac{(k_1 + c_1)}{2} \quad a_2 := \frac{(k_2 + c_2)}{2} \]

\[ a_1 = 0.764 \quad a_2 = 0.445 \]

Generic Transfer Function

\[ H_s = \frac{\left[ \alpha^2 s^2 + \beta \left( \frac{\omega_0}{Q} s \right) + \frac{\omega_0^2}{\alpha} \right]}{s^2 + \frac{\omega_0^2}{Q} (s) + \omega_0^2} \]

\[ \alpha := 2a - c \]

\[ \beta := 2b - c \]

\[ c := 2b \]
Setting Up Component Values

$$\text{Cap} := 10^{-9}$$

$$R_{1st1} := \frac{1}{\text{Cap} \cdot \omega_{01\text{Den}}}$$

$$R_{1st1} = 5.913 \times 10^4$$

$$R_{1st2} := Q_1 \cdot \frac{R_{1st1}}{b_1}$$

$$R_{1st2} = 8.309 \times 10^5$$

$$R_{1st3} := Q_1 \cdot \frac{R_{1st1}}{1 - b_1}$$

$$R_{1st3} = 3.25 \times 10^5$$

$$R_{1st4} := \frac{R_{1st1}}{c_1}$$

$$R_{1st4} = 1.052 \times 10^5$$

$$R_{1st5} := \frac{R_{1st1}}{1 - c_1}$$

$$R_{1st5} = 1.351 \times 10^5$$

$$C_{1st1} := a_1 \cdot \text{Cap}$$

$$C_{1st1} = 7.641 \times 10^{-9}$$

$$C_{1st2} := (1 - a_1) \cdot \text{Cap}$$

$$C_{1st2} = 2.359 \times 10^{-9}$$

$$R_{2nd1} := \frac{1}{\text{Cap} \cdot \omega_{02\text{Den}}}$$

$$R_{2nd1} = 2.448 \times 10^3$$

$$R_{2nd2} := Q_2 \cdot \frac{R_{2nd1}}{b_1}$$

$$R_{2nd2} = 3.44 \times 10^4$$

$$R_{2nd3} := Q_2 \cdot \frac{R_{2nd1}}{1 - b_2}$$

$$R_{2nd3} = 1.346 \times 10^4$$

$$R_{2nd4} := \frac{R_{2nd1}}{c_2}$$

$$R_{2nd4} = 4.354 \times 10^3$$

$$R_{2nd5} := \frac{R_{2nd1}}{1 - c_2}$$

$$R_{2nd5} = 5.593 \times 10^3$$

$$C_{2nd1} := a_2 \cdot \text{Cap}$$

$$C_{2nd1} = 4.446 \times 10^{-9}$$

$$C_{2nd2} := (1 - a_2) \cdot \text{Cap}$$

$$C_{2nd2} = 5.554 \times 10^{-9}$$
Appendix III: PSPICE Design

a) Low-Pass Notch Design

Output to Stage 2
Input from Stage 1
b) High-Pass Notch Design

Output to Stage 2
Input from Stage 1
c) Band-Pass Design

Output to Stage 2
Input from Stage 1
Appendix IV: Calculations for the MF10

a) Low-Pass Design

\( \omega_c := 200 \)

\[
\begin{align*}
R_{11} &:= 10 \cdot 10^3 \\
R_{12} &:= 10 \cdot 10^3 \\
R_{11} &:= 1 \times 10^4 \\
R_{12} &:= 1 \times 10^4 \\
R_{21} &:= R_{11} \\
R_{22} &:= R_{11} \\
R_{21} &:= 1 \times 10^4 \\
R_{22} &:= 1 \times 10^4 \\
f_{\text{CLK}} &:= \omega_c \cdot 100 \\
f_{\text{CLK}} &:= \omega_c \cdot 100 \\
f_{\text{CLK}} &:= 2 \times 10^4 \\
f_{\text{CLK}} &:= 2 \times 10^4 \\
Q_1 &:= 20.246 \\
Q_2 &:= 1.247 \\
f_{11} &:= \omega_{z1} \\
f_{11} &:= \omega_{z2} \\
f_{01} &:= f_{11} \cdot \omega_c \\
f_{01} &:= f_{11} \cdot \omega_c \\
f_{01} &:= 341.661 \\
f_{01} &:= 210.542
\end{align*}
\]
$$f_01 = \frac{f_{\text{CLK}}}{100} \left( \sqrt{\frac{R_{21}}{R_{41}}} + 1 \right) \quad \text{solve } R_{41} \rightarrow 5212.9489652296304024$$

$$Q_1 = \sqrt{\frac{R_{21}}{5212.9489652296304024 + 1}} \quad \text{solve } R_{31} \rightarrow 118513.96852074834742$$

$$f_02 = \frac{f_{\text{CLK}}}{100} \left( \sqrt{\frac{R_{22}}{R_{42}}} + 1 \right) \quad \text{solve } R_{42} \rightarrow 92421.441774491682034$$

$$Q_2 = \sqrt{\frac{R_{22}}{92421.441774491682034 + 1}} \quad \text{solve } R_{32} \rightarrow 11841.24471095798995$$
b) High-Pass Design

\[ \omega_c := 7 \times 10^3 \]
\[ R_{11} := 10 \times 10^3 \]
\[ R_{11} = 1 \times 10^4 \]
\[ R_{21} := R_{11} \]
\[ R_{21} = 1 \times 10^4 \]
\[ f_{CLK} := \omega_c / 50 \]
\[ f_{CLK} = 3.5 \times 10^5 \]
\[ Q1 = 0.751 \]
\[ f_{n1} = \omega_{z1} \]
\[ f_{n1} = 0.849 \]
\[ f_{01} := f_{n1} \cdot \omega_c \]
\[ f_{01} = 3.144 \times 10^3 \]
\[ f_{01} = \frac{f_{CLK}}{50} \left( \sqrt{\frac{R_{21}}{R_{41}}} \right) \]
\[ \text{solve} \quad R_{41} \rightarrow 49578.58205255326974 \]
\[ Q1 = \sqrt{\frac{R_{21}}{49578.58205255326974}} \left( \frac{R_{21}}{R_{31}} \right) \]
\[ \text{solve} \quad R_{31} \rightarrow 5976.822679576938799 \]
\[ f_{02} = \frac{f_{CLK}}{50} \left( \sqrt{\frac{R_{22}}{R_{42}}} \right) \]
\[ \text{solve} \quad R_{42} \rightarrow 13791.201213625706799 \]
\[ Q2 = \sqrt{\frac{R_{22}}{13791.201213625706799}} \left( \frac{R_{22}}{R_{32}} \right) \]
\[ \text{solve} \quad R_{32} \rightarrow 787.4443594868071794 \]
c) Band-Pass Design

\[ \omega_c := \sqrt{250 \cdot 7 \cdot 10^3} \]
\[ \omega_c = 1.323 \times 10^3 \]
\[ \text{R11} := 10 \cdot 10^3 \]
\[ \text{R11} = 1 \times 10^4 \]
\[ \text{R}_{21} := \text{R11} \]
\[ \text{R}_{21} = 1 \times 10^4 \]
\[ \text{fCLK} := \omega_c \times 50 \]
\[ \text{fCLK} = 6.614 \times 10^4 \]
\[ \text{Q1} = 3.951 \]
\[ \text{f}_{n1} := \omega_{z1} \]
\[ \text{f}_{n1} = 0.155 \]
\[ \text{f01} := \text{f}_{n1} \cdot \omega_c \]
\[ \text{f01} = 205.366 \]

\[ \text{R12} := 10 \cdot 10^3 \]
\[ \text{R12} = 1 \times 10^4 \]
\[ \text{R}_{22} := \text{R11} \]
\[ \text{R}_{22} = 1 \times 10^4 \]

\[ \text{Q2} = 3.951 \]
\[ \text{f}_{n2} := \omega_{z2} \]
\[ \text{f}_{n2} = 6.446 \]
\[ \text{f02} := \text{f}_{n2} \cdot \omega_c \]
\[ \text{f02} = 8.527 \times 10^3 \]
\[ f01 = \frac{fCLK}{50} \left( \sqrt{\frac{R_{21}}{R_{41}}} \right) \text{ solve } R_{41} \rightarrow 414937.75933609958505 \]

\[ Q1 = \sqrt{\frac{R_{21}}{414937.75933609958505}} \cdot \left( \frac{R_{21}}{R_{31}} \right) \text{ solve } R_{31} \rightarrow 392.93035424235699354 \]

\[ f02 = \frac{fCLK}{50} \left( \frac{R_{22}}{R_{42}} \right) \text{ solve } R_{42} \rightarrow 240.66983227719388601 \]

\[ Q2 = \sqrt{\frac{R_{22}}{240.669832227719388601}} \cdot \left( \frac{R_{22}}{R_{32}} \right) \text{ solve } R_{32} \rightarrow 16314.10205689667045 \]
Appendix V: MF10 Specification
Universal Monolithic Dual Switched Capacitor Filter

General Description

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages.

Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed. For pin-compatible device with improved performance refer to LMF100 datasheet.

Features
- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- f0 x Q range up to 200 kHz
- Operation up to 30 kHz
- 20-pin 0.3" wide Dual-In-Line package
- 20-pin Surface Mount (SO) wide-body package

System Block Diagram

Package in 20 pin molded wide body surface mount and 20 pin molded DIP.
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- **Supply Voltage (V⁺ – V⁻)**: 14V
- **Voltage at Any Pin**:
  - V⁺ + 0.3V
  - V⁻ – 0.3V
- **Input Current at Any Pin (Note 2)**: 5 mA
- **Package Input Current (Note 2)**: 20 mA
- **Power Dissipation (Note 3)**: 500 mW
- **Storage Temperature**: 150°C
- **ESD Susceptability (Note 11)**: 2000V

**Soldering Information**
- N Package: 10 sec 260°C
- SO Package:
  - Vapor Phase (60 Sec.) 215°C
  - Infrared (15 Sec.) 220°C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” (Appendix D) for other methods of soldering surface mount devices.

### Operating Ratings (Note 1)

<table>
<thead>
<tr>
<th>Temperature Range</th>
<th>T_MIN ≤ T_A ≤ T_MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>MF10ACN, MF10CCN</td>
<td>0°C ≤ T_A ≤ 70°C</td>
</tr>
<tr>
<td>MF10CCWM</td>
<td>0°C ≤ T_A ≤ 70°C</td>
</tr>
</tbody>
</table>

### Electrical Characteristics

- **V⁺ = +5.00V and V⁻ = −5.00V unless otherwise specified. Boldface limits apply for T_MIN to T_MAX; all other limits T_A = T_J = 25°C.**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>MF10ACN, MF10CCN, MF10CCWM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td><strong>Conditions</strong></td>
<td><strong>Typical (Note 8)</strong></td>
</tr>
<tr>
<td>V⁺ – V⁻</td>
<td><strong>Supply Voltage</strong></td>
<td>Min</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max</td>
<td>14</td>
</tr>
<tr>
<td>Iₛ</td>
<td><strong>Maximum Supply Current</strong></td>
<td>Clock Applied to Pins 10 &amp; 11 No Input Signal</td>
<td>8</td>
</tr>
<tr>
<td>fₒ</td>
<td><strong>Center Frequency Range</strong></td>
<td>Min fₒ x Q &lt; 200 kHz</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max</td>
<td>30</td>
</tr>
<tr>
<td>f_CLK</td>
<td><strong>Clock Frequency Range</strong></td>
<td>Min</td>
<td>5.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max</td>
<td>1.5</td>
</tr>
<tr>
<td>f_CLK/fₒ</td>
<td><strong>50:1 Clock to Center Frequency Ratio Deviation</strong></td>
<td>Q = 10 Mode 1 V_pin12 = 5V f_clk = 250 kHz</td>
<td>±0.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q = 10 Mode 1 V_pin12 = 0V f_clk = 500 kHz</td>
<td>±0.2</td>
</tr>
<tr>
<td>Clock Feedthrough</td>
<td><strong>50:1 Clock to Center Frequency Ratio Deviation</strong></td>
<td>Q = 10 Mode 1 V_pin12 = 5V f_clk = 250 kHz</td>
<td>±0.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q = 10 Mode 1 V_pin12 = 0V f_clk = 500 kHz</td>
<td>±0.2</td>
</tr>
<tr>
<td>Q Error (MAX)</td>
<td><strong>Q Error (MAX)</strong> (Note 4)</td>
<td>Q = 10 Mode 1 V_pin12 = 5V f_clk = 250 kHz</td>
<td>±2</td>
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<tr>
<td></td>
<td></td>
<td>V_pin12 = 0V f_clk = 500 kHz</td>
<td>±2</td>
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<tr>
<td>H_CLP</td>
<td><strong>DC Lowpass Gain</strong></td>
<td>Mode 1 R1 = R2 = 10k</td>
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<tr>
<td>V_OS1</td>
<td><strong>DC Offset Voltage (Note 5)</strong></td>
<td>Min</td>
<td>±5.0</td>
</tr>
<tr>
<td>V_OS2</td>
<td><strong>DC Offset Voltage</strong></td>
<td>Min</td>
<td>V_pin12 = +5V S_AB = V⁺</td>
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</table>
### Electrical Characteristics (Continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>MF10ACN, MF10CCN, MF10CCWM</th>
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</thead>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Typical</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Limit</td>
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<td></td>
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<td>(Note 8)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Max (f CLK/f O = 50)</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Min V pin12 = +5V</td>
</tr>
<tr>
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<td>Max V pin12 = +5V</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Min V pin12 = +5V</td>
</tr>
<tr>
<td>V OS3</td>
<td>DC Offset Voltage</td>
<td>Min V pin12 = +5V</td>
<td>−70</td>
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<tr>
<td></td>
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<td>Max V pin12 = +5V</td>
<td>−20</td>
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<tr>
<td>V OS2</td>
<td>DC Offset Voltage</td>
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<td>Max V pin12 = 0V</td>
<td>−140</td>
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<td>V OS3</td>
<td>DC Offset Voltage</td>
<td>Min V pin12 = 0V</td>
<td>−140</td>
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<tr>
<td>V OUT</td>
<td>Minimum Output Voltage Swing</td>
<td>BP, LP Pins</td>
<td>±4.25</td>
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<td></td>
<td>N/AP/HP Pins</td>
<td>±4.25</td>
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<tr>
<td>GBW</td>
<td>Op Amp Gain BW Product</td>
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<td>SR</td>
<td>Op Amp Slew Rate</td>
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<td>Dynamic Range (Note 6)</td>
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<td>ISC</td>
<td>Maximum Output Short Source</td>
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<tr>
<td></td>
<td>Circuit Current</td>
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<td>3.0</td>
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</table>

### Logic Input Characteristics

**Boldface limits apply for T MIN to T MAX:** all other limits T A = T J = 25°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>MF10ACN, MF10CCN, MF10CCWM</th>
</tr>
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<tbody>
<tr>
<td></td>
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<td>Typical</td>
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<td>Limit</td>
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<td>(Note 8)</td>
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<tr>
<td>CMOS Clock Input Voltage</td>
<td>Min Logical “1” V + = +5V, V − = −5V,</td>
<td>+3.0</td>
</tr>
<tr>
<td></td>
<td>Max Logical “0” V LSN = 0V</td>
<td>−3.0</td>
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<tr>
<td></td>
<td>Min Logical “1” V + = +10V, V − = 0V,</td>
<td>+8.0</td>
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<tr>
<td></td>
<td>Max Logical “0” V LSN = +5V</td>
<td>+2.0</td>
</tr>
<tr>
<td>TTL Clock Input Voltage</td>
<td>Min Logical “1” V + = +5V, V − = −5V,</td>
<td>+2.0</td>
</tr>
<tr>
<td></td>
<td>Max Logical “0” V LSN = 0V</td>
<td>+0.8</td>
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</table>
### Logic Input Characteristics (Continued)

**Boldface limits apply for** $T_{\text{MIN}}$ to $T_{\text{MAX}}$; all other limits $T_A = T_J = 25^\circ\text{C}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>MF10ACN, MF10CCN, MF10CCWM</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min Logical &quot;1&quot;</td>
<td>$V^+ = +10\text{V}, V^- = 0\text{V}$</td>
<td>Typical (Note 8)</td>
<td>Tested Limit (Note 9)</td>
</tr>
<tr>
<td>Max Logical &quot;0&quot;</td>
<td>$V_{\text{LSH}} = 0\text{V}$</td>
<td>+2.0</td>
<td>+2.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>+0.8</td>
<td>+0.8</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** When the input voltage ($V_{\text{IN}}$) at any pin exceeds the power supply rails ($V_{\text{IN}} < V^- \text{ or } V_{\text{IN}} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

**Note 3:** The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{\text{JMAX}}, \theta JA,$ and the ambient temperature, $T_A$. The maximum allowable power dissipation at any temperature is $P_D = (T_{\text{JMAX}} - T_A)/\theta JA$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{\text{JMAX}} = 125^\circ\text{C}$, and the typical junction-to-ambient thermal resistance of the MF10ACN/CCN when board mounted is 55$^\circ\text{C/W}$. For the MF10AC/CCJ, this number increases to 95$^\circ\text{C/W}$ and for the MF10ACWM/CCWM this number is 66$^\circ\text{C/W}$.

**Note 4:** The accuracy of the $Q$ value is a function of the center frequency ($f_0$). This is illustrated in the curves under the heading “Typical Performance Characteristics”.

**Note 5:** $V_{\text{OS1}}, V_{\text{OS2}},$ and $V_{\text{OS3}}$ refer to the internal offsets as discussed in the Applications Information Section 3.4.

**Note 6:** For ±5V supplies the dynamic range is referenced to 2.82V rms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200$\mu\text{V}$ rms for the MF10 with a 50:1 CLK ratio and 280$\mu\text{V}$ rms for the MF10 with a 100:1 CLK ratio.

**Note 7:** The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

**Note 8:** Typicals are at 25$^\circ\text{C}$ and represent most likely parametric norm.

**Note 9:** Tested limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

**Note 10:** Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

**Note 11:** Human body model, 100 pF discharged through a 1.5 k$\Omega$ resistor.
Typical Performance Characteristics (Continued)

Q Deviation vs. Temperature

- $V_S = \pm 5V$
- NOMINAL $Q = 10.0$
- MODE 1
- $f_{CLK} = 500$ kHz
- $f_{CLK} / f_O = 100:1$

Q Deviation vs. Temperature

- $V_S = \pm 5V$
- NOMINAL $Q = 10.0$
- MODE 1
- $f_{CLK} = 250$ kHz
- $f_{CLK} / f_O = 50:1$

Q Deviation vs. Clock Frequency

- $V_S = \pm 5V$
- $T_A = 25^\circ C$
- NOMINAL $Q = 10.0$
- MODE 1
- $f_{CLK} / f_O = 100:1$

Q Deviation vs. Clock Frequency

- $V_S = \pm 5V$
- $T_A = 25^\circ C$
- NOMINAL $Q = 10.0$
- MODE 1
- $f_{CLK} / f_O = 50:1$

$f_{CLK}/f_O$ Deviation vs. Temperature

- $V_S = \pm 5V$
- NOMINAL $Q = 10.0$
- MODE 1
- $f_{CLK} = 500$ kHz
- $f_{CLK} / f_O = 100:1$

$f_{CLK}/f_O$ Deviation vs. Temperature

- $V_S = \pm 5V$
- NOMINAL $Q = 10.0$
- MODE 1
- $f_{CLK} = 250$ kHz
- $f_{CLK} / f_O = 50:1$
Typical Performance Characteristics (Continued)

**f\textsubscript{CLK}/f\textsubscript{O} Deviation vs. Clock Frequency**

% CHANGE

0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
-0.05
-0.10
-0.15
-0.20
-0.25
-0.30
-0.35
-0.40

100 200 300 400 500 600 700 800 900 1000

CLOCK FREQUENCY (kHz)

**Deviation of f\textsubscript{CLK}/f\textsubscript{O} vs. Nominal Q**

V\textsubscript{S} = ±5V
T\textsubscript{A} = 25°C

Nominal Q = 10.0
Mode 1

f\textsubscript{CLK} = 100:1
f\textsubscript{O} = 1

% CHANGE

0.5
0.4
0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3
-0.4
-0.5

0.1 1.0 10 100

Nominal Q

01039948

01039947

01039949

01039948

www.national.com
Pin Descriptions

LP(1,20), BP(2,19), N/AP/HP(3,18)
The second order lowpass, bandpass and notch/allpass/highpass outputs. These outputs can typically sink 1.5 mA and source 3 mA. Each output typically swings to within 1V of each supply.

INV(4,17)The inverting input of the summing op-amp of each filter. These are high impedance inputs, but the non-inverting input is internally tied to AGND, making INV<sub>a</sub> and INV<sub>b</sub> behave like summing junctions (low impedance, current inputs).

S1(5,16)S1 is a signal input pin used in the allpass filter configurations (see modes 4 and 5). The pin should be driven with a source impedance of less than 1 kΩ. If S1 is not driven with a signal it should be tied to AGND (mid-supply).

S<sub>a/b</sub>(6)This pin activates a switch that connects one of the inputs of each filter’s second summer to either AGND (S<sub>a/b</sub> tied to V<sub>−</sub>) or to the lowpass (LP) output (S<sub>a/b</sub> tied to V<sub>+</sub>). This offers the flexibility needed for configuring the filter in its various modes of operation.

V<sub>a</sub>+(7), V<sub>d</sub>+(8)Analog positive supply and digital positive supply. These pins are internally connected through the IC substrate and therefore V<sub>a</sub>+ and V<sub>d</sub>+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.

V<sub>a</sub>−(14), V<sub>d</sub>−(13)Analog and digital negative supplies. The same comments as for V<sub>a</sub>+ and V<sub>d</sub>+ apply here.

LSh(9)Level shift pin; it accommodates various clock levels with dual or single supply operation. With dual ±5V supplies, the MF10 can be driven with CMOS clock levels (±5V) and the LSh pin should be tied to the system ground. If the same supplies as above are used but only TTL clock levels, derived from 0V to +5V supply, are available, the LSh pin should be tied to the system ground.

1.0 Definition of Terms

f<sub>CLK</sub>: the frequency of the external clock signal applied to pin 10 or 11.

f<sub>o</sub>: center frequency of the second order function complex pole pair. f<sub>o</sub> is measured at the bandpass outputs of the MF10, and is the frequency of maximum bandpass gain. (Figure 1)

f<sub>notch</sub>: the frequency of minimum (ideally zero) gain at the notch outputs.

f<sub>z</sub>: the center frequency of the second order complex zero pair, if any. If f<sub>z</sub> is different from f<sub>o</sub> and if Q<sub>z</sub> is high, it can be observed as the frequency of a notch at the allpass output. (Figure 10)

Q: “quality factor” of the 2nd order filter. Q is measured at the bandpass outputs of the MF10 and is equal to f<sub>o</sub> divided by the −3 dB bandwidth of the 2nd order bandpass filter (Figure f). The value of Q determines the shape of the 2nd order filter responses as shown in Figure 6.

Q<sub>z</sub>: the quality factor of the second order complex zero pair, if any. Q<sub>z</sub> is related to the allpass characteristic, which is written:

\[ H_{AP}(s) = \frac{H_{OBP}(s^2 - \frac{8\omega Q}{Q^2} + \omega^2)}{s^2 + \frac{8\omega Q}{Q} + \omega^2} \]

where Q<sub>z</sub> = Q for an all-pass response.

H<sub>OBP</sub>: the gain (in V/V) of the bandpass output at f = f<sub>o</sub>.
1.0 Definition of Terms (Continued)

$H_{OLP}$: the gain (in V/V) of the lowpass output as $f \to 0$ Hz (Figure 2).

$H_{OHP}$: the gain (in V/V) of the highpass output as $f \to f_{CLK}/2$ (Figure 3).

$H_{ON}$: the gain (in V/V) of the notch output as $f \to 0$ Hz and as $f \to f_{CLK}/2$, when the notch filter has equal gain above and below the center frequency (Figure 4). When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a (Figure 11 and Figure 8), the two quantities below are used in place of $H_{ON}$.

$H_{ON1}$: the gain (in V/V) of the notch output as $f \to 0$ Hz.

$H_{ON2}$: the gain (in V/V) of the notch output as $f \to f_{CLK}/2$.

\[
H_{BP}(s) = \frac{H_{OHP} \omega_0 S}{s^2 + \frac{8 \omega_0}{Q} + \omega_0^2}
\]

\[
Q = \frac{f_0}{f_H - f_L}, \quad f_0 = \frac{f_{CLK}}{2}
\]

\[
f_L = f_0 \left( \frac{-1}{2Q} + \sqrt{\frac{1}{4Q^2} + 1} \right)
\]

\[
f_H = f_0 \left( \frac{1}{2Q} + \sqrt{\frac{1}{4Q^2} + 1} \right)
\]

\[
\omega_0 = 2\pi f_0
\]

FIGURE 1. 2nd-Order Bandpass Response
1.0 Definition of Terms (Continued)

\[ H_{LP}(s) = \frac{H_{OLP} s^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \]

\[ f_c = f_0 \sqrt{1 - \frac{1}{2Q^2}} + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1} \]

\[ f_p = f_0 \sqrt{1 - \frac{1}{2Q^2}} \]

\[ H_{OP} = H_{OLP} \times \frac{1}{\delta \sqrt{1 - \frac{1}{4Q^2}}} \]

FIGURE 2. 2nd-Order Low-Pass Response
1.0 Definition of Terms (Continued)

\[ H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + \frac{s\omega_Q}{Q} + \omega_Q^2} \]

\[ f_c = f_0 \times \left[ \sqrt{1 - \frac{1}{2Q^2}} + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1} \right]^{-1} \]

\[ f_p = f_0 \times \left[ \sqrt{1 - \frac{1}{2Q^2}} \right]^{-1} \]

\[ H_{OP} = H_{OHP} \times \frac{1}{Q \sqrt{1 - \frac{1}{4Q^2}}} \]

FIGURE 3. 2nd-Order High-Pass Response
1.0 Definition of Terms (Continued)

![Diagram of 2nd-Order Notch Response](image)

\[ H_N(s) = \frac{H_{DN}(s^2 + \omega_0^2)}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2} \]

\[ Q = \frac{f_0}{f_H - f_L}, \quad f_0 = \frac{f_L f_H}{f_H - f_L} \]

\[ f_L = f_0 \left( \frac{-1}{2Q} + \sqrt{\frac{1}{2Q}} + 1 \right) \]

\[ f_H = f_0 \left( \frac{1}{2Q} + \sqrt{\frac{1}{2Q}} + 1 \right) \]

FIGURE 4. 2nd-Order Notch Response
1.0 Definition of Terms (Continued)

![Diagram of 2nd-Order All-Pass Response](image)

**FIGURE 5. 2nd-Order All-Pass Response**

\[
H_{AP}(s) = \frac{H_{OAP} \left( s^2 - \frac{s\omega_0}{Q} + \omega_0^2 \right)}{s^2 + \frac{s\omega_0}{Q} + \omega_0^2}
\]
2.0 Modes of Operation

The MF10 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain approach is appropriate. Since this is cumbersome, and since the MF10 closely approximates continuous filters, the following discussion is based on the well known frequency domain. Each MF10 can produce a full 2nd order function. See Table 1 for a summary of the characteristics of the various modes.

**MODE 1: Notch 1, Bandpass, Lowpass Outputs:**

\[ f_{\text{notch}} = f_0 \text{ (See Figure 7)} \]

\[ f_0 = \text{center frequency of the complex pole pair} \]

\[ f_{\text{notch}} = \text{center frequency of the imaginary zero pair} = f_0. \]

\[ H_{\text{OLP}} = \text{Lowpass gain (as } f \to 0) = -\frac{R_2}{R_1} \]

\[ H_{\text{OBP}} = \text{Bandpass gain (at } f = f_0) = -\frac{R_3}{R_1} \]

\[ H_{\text{ON}} = \text{Notch output gain as } f \to 0, f \to f_{\text{CLK/2}} = -\frac{R_2}{R_1} \]

**Note:** \( V_{\text{IN}} \) should be driven from a low impedance (<1 kΩ) source.

\[ Q = \frac{f_0}{BW} = \frac{R_3}{R_2} \]

= quality factor of the complex pole pair

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

\[ H_{\text{OLP}} = \frac{H_{\text{OBP}}}{Q} \text{ or } H_{\text{OBP}} = H_{\text{OLP}} \times Q \]

\[ = H_{\text{ON}} \times Q. \]

\[ H_{\text{OLP(peak)}} = Q \times H_{\text{OLP}} \text{ (for high } Q \text{'s)} \]

**MODE 1a: Non-Inverting BP, LP (See Figure 8)**

\[ f_0 = \frac{f_{\text{CLK}}}{100} \text{ or } \frac{f_{\text{CLK}}}{50} \]

\[ Q = \frac{R_3}{R_2} \]

\[ H_{\text{OLP}} = -1; H_{\text{OLP(peak)}} = Q \times H_{\text{OLP}} \text{ (for high } Q \text{'s)} \]

\[ H_{\text{OBP}} = -\frac{R_3}{R_2} \]

\[ H_{\text{OBP}} = 1 \text{ (Non-Inverting)} \]

Circuit Dynamics: \( H_{\text{OBP}} = Q \)
2.0 Modes of Operation  (Continued)

MODE 2: Notch 2, Bandpass, Lowpass:  \( f_{\text{notch}} < f_o \)

(See Figure 9)

\[
\begin{align*}
  f_o &= \text{center frequency} \\
  &= \frac{f_{\text{CLK}} \sqrt{R_2}}{100} + 1 \quad \text{or} \quad \frac{f_{\text{CLK}} \sqrt{R_2}}{50} + 1 \\
  f_{\text{notch}} &= \frac{f_{\text{CLK}}}{100} \quad \text{or} \quad \frac{f_{\text{CLK}}}{50} \\
  Q &= \text{quality factor of the complex pole pair} \\
  &= \frac{\sqrt{R_2/R_4 + 1}}{R_2/R_3} \\
  H_{\text{OLP}} &= \text{Lowpass output gain (as } f \to 0) \\
  &= -\frac{R_2/R_1}{R_2/R_4 + 1} \\
  H_{\text{OBP}} &= \text{Bandpass output gain (at } f = f_o) = -\frac{R_3}{R_1} \\
  H_{\text{ON1}} &= \text{Notch output gain (at } f \to 0) \\
  &= -\frac{R_2/R_1}{R_2/R_4 + 1} \\
  H_{\text{ON2}} &= \text{Notch output gain (as } f \to \frac{f_{\text{CLK}}}{2}) = -\frac{R_2}{R_1} \\
  \text{Filter dynamics: } H_{\text{OBP}} &= Q \sqrt{H_{\text{OLP}} H_{\text{ON2}}} = \sqrt{H_{\text{ON1}} H_{\text{ON2}}} \\
  \text{Circuit dynamics: } R_2 &= H_{\text{OLP}} \quad \text{or} \quad R_4 = H_{\text{HOP}} \\
  H_{\text{OBP}} &= \sqrt{H_{\text{OLP}} H_{\text{HOP}}} \times Q \\
  H_{\text{OLP(peak)}} &= Q \times H_{\text{OLP}} \text{ (for high } Q's) \\
  H_{\text{HOP(peak)}} &= Q \times H_{\text{HOP}} \text{ (for high } Q's)
\end{align*}
\]

MODE 3: Highpass, Bandpass, Lowpass Outputs

(See Figure 10)

\[
\begin{align*}
  f_o &= \frac{f_{\text{CLK}} \sqrt{R_2}}{100} \quad \text{or} \quad \frac{f_{\text{CLK}} \sqrt{R_2}}{50} \quad \text{or} \quad \frac{R_2}{R_4} \quad \text{or} \quad \frac{R_2}{R_4} \\
  Q &= \text{quality factor of the complex pole pair} \\
  &= \frac{\sqrt{R_2/R_3}}{\sqrt{R_4}} \\
  H_{\text{HOP}} &= \text{Highpass Gain (as } f \to \frac{f_{\text{CLK}}}{2}) = -\frac{R_2}{R_1} \\
  H_{\text{OBP}} &= \text{Lowpass Gain (at } f = f_o) = -\frac{R_3}{R_1} \\
  H_{\text{OLP}} &= \text{Lowpass Gain (as } f \to 0) = -\frac{R_4}{R_1} \\
  \text{Circuit dynamics: } R_2 &= H_{\text{HOP}} \quad \text{or} \quad R_4 = H_{\text{OLP}} \\
  H_{\text{OBP}} &= \sqrt{H_{\text{HOP}} H_{\text{OLP}}} \times Q \\
  H_{\text{OLP(peak)}} &= Q \times H_{\text{OLP}} \text{ (for high } Q's) \\
  H_{\text{HOP(peak)}} &= Q \times H_{\text{HOP}} \text{ (for high } Q's)
\end{align*}
\]

FIGURE 7. MODE 1

FIGURE 8. MODE 1a
2.0 Modes of Operation (Continued)

*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF – 100 pF) across R4 to provide some phase lead.
2.0 Modes of Operation (Continued)

MODE 3a: HP, BP, LP and Notch with External Op Amp (See Figure 11)

\[ f_0 = \frac{f_{CLK}}{100} \sqrt{\frac{R_2}{R_4}} \text{ or } \frac{f_{CLK}}{50} \sqrt{\frac{R_2}{R_4}} \]

\[ Q = \sqrt{\frac{R_2}{R_4} \times \frac{R_3}{R_2}} \]

\[ H_{OHP} = \frac{R_2}{R_1} \]

\[ H_{OBP} = \frac{R_3}{R_1} \]

\[ H_{OLP} = \frac{R_4}{R_1} \]

\[ f_n = \text{notch frequency} = \frac{f_{CLK}}{100} \sqrt{\frac{R_h}{R_i}} \text{ or } \frac{f_{CLK}}{50} \sqrt{\frac{R_h}{R_i}} \]

\[ H_{ON} = \text{gain of notch at } f = f_0 = \left| Q \left( \frac{R_i}{R_h} H_{OLP} - \frac{R_h}{R_i} H_{OHP} \right) \right| \]

\[ H_{n1} = \text{gain of notch (as } f \rightarrow 0) = \frac{R_i}{R_h} \times H_{OLP} \]

\[ H_{n2} = \text{gain of notch (as } f \rightarrow \frac{f_{CLK}}{2}) \]

\[ = \frac{R_i}{R_h} \times H_{OHP} \]

MODE 4: Allpass, Bandpass, Lowpass Outputs (See Figure 12)

\[ f_0 = \text{center frequency} \]

\[ = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50} \]

\[ Q = \frac{f_0}{BW} = \frac{R_3}{R_2} \]

\[ Q_2 = \text{quality factor of complex zero pair} = \frac{R_3}{R_1} \]

For AP output make \( R_1 = R_2 \)

\[ H_{OAP} = \text{Allpass gain (at } 0 < f < \frac{f_{CLK}}{2}) = \frac{R_2}{R_1} = -1 \]

\[ H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0) \]

\[ = - \left( \frac{R_2}{R_1} + 1 \right) = -2 \]

\[ H_{OBP} = \text{Bandpass gain (at } f = f_0) \]

\[ = - \frac{R_3}{R_2} \left( 1 + \frac{R_2}{R_1} \right) = -2 \left( \frac{R_3}{R_2} \right) \]

Circuit Dynamics: \( H_{OAP} \times (H_{OLP} + 1)Q \)

*Due to the sampled data nature of the filter, a slight mismatch of \( f_n \) and \( f_0 \) occurs causing a 0.4 dB peaking around \( f_0 \) of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

FIGURE 11. MODE 3a
2.0 Modes of Operation  

(Continued)

**MODE 5: Numerator Complex Zeros, BP, LP**  
(See Figure 13)

\[
f_0 = \sqrt{1 + \frac{R_2}{R_4} \times \frac{f_{CLK}}{100}} \text{ or } \sqrt{1 + \frac{R_2}{R_4} \times \frac{f_{CLK}}{50}}
\]

\[
f_z = \sqrt{1 - \frac{R_2}{R_4} \times \frac{f_{CLK}}{100}} \text{ or } \sqrt{1 - \frac{R_1}{R_4} \times \frac{f_{CLK}}{50}}
\]

\[Q = \sqrt{1 + \frac{R_2}{R_4} \times \frac{R_3}{R_2}}
\]

\[Q_z = \sqrt{1 - \frac{R_1}{R_4} \times \frac{R_3}{R_1}}
\]

\[H_{021} = \text{gain at C.Z. output (as } f \rightarrow 0 \text{ Hz)}\]

\[H_{022} = \text{gain at C.Z. output (as } f \rightarrow \frac{f_{CLK}}{2}) = -\frac{R_2}{R_1}
\]

**MODE 6a: Single Pole, HP, LP Filter** (See Figure 14)

\[f_c = \text{cutoff frequency of LP or HP output}
\]

\[f_c = \frac{R_2}{R_3} \times \frac{f_{CLK}}{100}\]

\[H_{OLP} = -\frac{R_3}{R_1}
\]

\[H_{OHP} = -\frac{R_2}{R_1}
\]

**MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting)** (See Figure 15)

\[f_c = \text{cutoff frequency of LP outputs}
\]

\[f_c = \frac{R_2}{R_3} \times \frac{f_{CLK}}{100}\]

\[H_{OLP1} = 1 \text{ (non-inverting)}
\]

\[H_{OLP2} = -\frac{R_3}{R_2}
\]

---

**FIGURE 12. MODE 4**

**FIGURE 13. MODE 5**
### 2.0 Modes of Operation

(Continued)

TABLE 1. Summary of Modes. Realizable filter types (e.g. low-pass) denoted by asterisks. Unless otherwise noted, gains of various filter outputs are inverting and adjustable by resistor ratios.

<table>
<thead>
<tr>
<th>Mode</th>
<th>BP</th>
<th>LP</th>
<th>HP</th>
<th>N</th>
<th>AP</th>
<th>Number of Adjustable Resistors</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td></td>
<td>3</td>
<td>No</td>
</tr>
<tr>
<td>1a</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(2)</td>
<td>H\textsubscript{OBP1} = +Q  \text{ or } H\textsubscript{OBP2} = +1</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>May need input buffer. Poor dynamics for high Q.</td>
</tr>
<tr>
<td>2</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td></td>
<td>3</td>
<td>Yes (above ( f_{\text{CLK}}/50 ) or ( f_{\text{CLK}}/100 ))</td>
</tr>
<tr>
<td>3</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td></td>
<td>4</td>
<td>Yes Universal State-Variable Filter. Best general-purpose mode.</td>
</tr>
<tr>
<td>3a</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td></td>
<td>7</td>
<td>Yes As above, but also includes resistor-tuneable notch.</td>
</tr>
<tr>
<td>4</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td></td>
<td>3</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Gives Allpass response with ( H\text{AP} = -1 ) and ( H\text{OLP} = -2 ).</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td></td>
<td>4</td>
<td>Gives flatter allpass response than above if ( R_1 = R_2 = 0.02R_4 ).</td>
</tr>
<tr>
<td>6a</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td></td>
<td></td>
<td>3</td>
<td>Single pole.</td>
</tr>
<tr>
<td>6b</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(2)</td>
<td>H\textsubscript{OLP1} = -R3/\text{R2}</td>
<td>2</td>
</tr>
</tbody>
</table>

FIGURE 14. MODE 6a

FIGURE 15. MODE 6b
3.0 Applications Information

The MF10 is a general-purpose dual second-order state variable filter whose center frequency is proportional to the frequency of the square wave applied to the clock input (fCLK). By connecting pin 12 to the appropriate DC voltage, the filter center frequency fC can be made equal to either fCLK/100 or fCLK/50. fC can be very accurately set (within ±6%) by using a crystal clock oscillator, or can be easily varied over a wide frequency range by adjusting the clock frequency. If desired, the fCLK/fC ratio can be altered by external resistors as in Figures 9, 10, 11, 13, 14, 15. The filter Q and gain are determined by external resistors. All of the five second-order filter types can be built using either section of the MF10. These are illustrated in Figure 1 through Figure 5 along with their transfer functions and some related equations. Figure 6 shows the effect of Q on the shapes of these curves. When filter orders greater than two are desired, two or more MF10 sections can be cascaded.

3.1 DESIGN EXAMPLE

In order to design a second-order filter section using the MF10, we must define the necessary values of three parameters: f0, the filter section’s center frequency; H0, the passband gain; and the filter’s Q. These are determined by the characteristics required of the filter being designed.

As an example, let’s assume that a system requires a fourth-order Chebyshev low-pass filter with 1 dB ripple, unity gain at DC, and 1000 Hz cutoff frequency. As the system order is four, it is realizable using both second-order sections of an MF10. Many filter design texts include tables that list the characteristics (f0 and Q) of each of the second-order filter sections needed to synthesize a given higher-order filter. For the Chebyshev filter defined above, such a table yields the following characteristics:

f0A = 529 Hz  QA = 0.785
f0B = 993 Hz  QB = 3.559

For unity gain at DC, we also specify:

H0A = 1
H0B = 1

The desired clock-to-cutoff-frequency ratio for the overall filter of this example is 100 and a 100 kHz clock signal is available. Note that the required center frequencies for the two second-order sections will not be obtainable with clock-to-center-frequency ratios of 50 or 100. It will be necessary to adjust externally. From Table 1, we see that Mode 3 can be used to produce a low-pass filter with resistor-adjustable center frequency.

In most filter designs involving multiple second-order stages, it is best to place the stages with lower Q values ahead of stages with higher Q, especially when the higher Q is greater than 0.707. This is due to the higher relative gain at the center frequency of a higher-Q stage. Placing a stage with lower Q ahead of a higher-Q stage will provide some attenuation at the center frequency and thus help avoid clipping of signals near this frequency. For this example, stage A has the lower Q (0.785) so it will be placed ahead of the other stage.

For the first section, we begin the design by choosing a convenient value for the input resistance: R1A = 20k. The absolute value of the passband gain HCLPA is made equal to 1 by choosing R4A such that: R4A = −HCLPA R1A = R1A = 20k. If the 50/100/CL pin is connected to mid-supply for nominal 100:1 clock-to-center-frequency ratio, we find R2A by:

\[ R2A = R4A \times \frac{f0A^2}{(fCLK/100)^2} = 2 \times 10^4 \times \frac{(529)^2}{(1000)^2} = 5.6k \text{ and} \]
\[ R3A = QA \times R2A R4A = 0.785 \times 5.6 \times 10^3 \times 2 \times 10^4 = 6.3k \]

The resistors for the second section are found in a similar fashion:

R1B = 20k
R4B = R1B = 20k
R2B = R4B \times \frac{f0B^2}{(fCLK/100)^2} = 20k \times \frac{(993)^2}{(1000)^2} = 19.7k
R3B = QB \times R2B R4B = 3.559 \times 19.7 \times 10^3 \times 2 \times 10^4 = 70.6k

The complete circuit is shown in Figure 16 for split ±5V power supplies. Supply bypass capacitors are highly recommended.
FIGURE 16. Fourth-Order Chebyshev Low-Pass Filter from Example in 3.1. ±5V Power Supply. 0V–5V TTL or −5V ±5V CMOS Logic Levels.

3.0 Applications Information (Continued)

(a) Resistive Divider with Decoupling Capacitor

(b) Voltage Regulator

(c) Operational Amplifier with Divider

FIGURE 18. Three Ways of Generating V+\(/2\) for Single-Supply Operation
3.0 Applications Information

(Continued)

3.2 SINGLE SUPPLY OPERATION

The MF10 can also operate with a single-ended power supply. Figure 17 shows the example filter with a single-ended power supply. $V_{A+}$ and $V_{D+}$ are again connected to the positive power supply (8V to 14V), and $V_{A-}$ and $V_{D-}$ are connected to ground. The $AGND$ pin must be tied to $V^+$/2 for single supply operation. This half-supply point should be very “clean”, as any noise appearing on it will be treated as an input to the filter. It can be derived from the supply voltage with a pair of resistors and a bypass capacitor (Figure 18a), or a low-impedance half-supply voltage can be made using a three-terminal voltage regulator or an operational amplifier (Figure 18b and Figure 18c). The passive resistor divider with a bypass capacitor is sufficient for many applications, provided that the time constant is long enough to reject any power supply noise. It is also important that the half-supply reference present a low impedance to the clock frequency, so at very low clock frequencies the regulator or op-amp approaches may be preferable because they will require smaller capacitors to filter the clock frequency. The main power supply voltage should be clean (preferably regulated) and bypassed with 0.1 µF.

3.3 DYNAMIC CONSIDERATIONS

The maximum signal handling capability of the MF10, like that of any active filter, is limited by the power supply voltages used. The amplifiers in the MF10 are able to swing to within about 1V of the supplies, so the input signals must be kept small enough that none of the outputs will exceed these limits. If the MF10 is operating on ±5V, for example, the outputs will clip at about 8 $V_{P-P}$. The maximum input voltage multiplied by the filter gain should therefore be less than 8 $V_{P-P}$.

Note that if the filter Q is high, the gain at the lowpass or highpass outputs will be much greater than the nominal filter gain (Figure 6). As an example, a lowpass filter with a Q of 10 will have a 20 dB peak in its amplitude response at $f_o$. If the nominal gain of the filter $H_{LP}$ is equal to 1, the gain at $f_o$ will be 10. The maximum input signal at $f_o$ must therefore be less than 800 mV $V_{P-P}$ when the circuit is operated on ±5V supplies.

Also note that one output can have a reasonable small voltage on it while another is saturated. This is most likely for a circuit such as the notch in Mode 1 (Figure 7). The notch output will be very small at $f_o$, so it might appear safe to apply a large signal to the input. However, the bandpass will have its maximum gain at $f_o$, and can clip if overdriven. If one output clips, the performance at the other outputs will be degraded, so avoid overdriving any filter section, even ones whose outputs are not being directly used. Accompanying Figure 7 through Figure 15 are equations labeled “circuit dynamics”, which relate the Q and the gains at the various outputs. These should be consulted to determine peak circuit gains and maximum allowable signals for a given application.

3.4 OFFSET VOLTAGE

The MF10’s switched capacitor integrators have a higher equivalent input offset voltage than would be found in a typical continuous-time active filter integrator. Figure 19 shows an equivalent circuit of the MF10 from which the output DC offsets can be calculated. Typical values for these offsets with $SA/B$ tied to $V^+$ are:

$V_{os1} = \text{opamp offset} = \pm 5 \text{ mV}$

$V_{os2} = -150 \text{ mV @ 50:1}: -300 \text{ mV @ 100:1}$

$V_{os3} = -70 \text{ mV @ 50:1}: -140 \text{ mV @ 100:1}$

When $SA/B$ is tied to $V^-$, $V_{os2}$ will approximately halve. The DC offset at the BP output is equal to the input offset of the lowpass integrator ($V_{os3}$). The offsets at the other outputs depend on the mode of operation and the resistor ratios, as described in the following expressions.

**Mode 1 and Mode 4**

$$V_{OS(N)} = V_{OS1} \left( \frac{1}{Q} + 1 \left| H_{OLP} \right| \right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

**Mode 1a**

$$V_{OS(N.INV.BP)} = \left( 1 + \frac{1}{Q} \right) V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$$
3.0 Applications Information

(Continued)

Mode 2 and Mode 5

\[ V_{OS(N)} = \left( \frac{R_2}{R_p} + 1 \right) V_{OS1} \times \frac{1}{1 + \frac{R_2}{R_4}} \]

\[ + V_{OS2} \frac{1}{1 + \frac{R_4}{R_2}} - \frac{V_{OS3}}{Q(1 + \frac{R_2}{R_4})} ; \]

\[ R_p = \frac{R_1}{R_3} // R_4 \]

\[ V_{OS(BP)} = V_{OS3} \]

\[ V_{OS(LP)} = V_{OS(N)} - V_{OS2} \]

Mode 3

\[ V_{OS(HP)} = V_{OS2} \]

\[ V_{OS(BP)} = V_{OS3} \]

\[ V_{OS(LP)} = V_{OS1} \left( 1 + \frac{R_4}{R_p} \right) - V_{OS2} \left( \frac{R_4}{R_2} \right) \]

\[ - V_{OS3} \left( \frac{R_4}{R_3} \right) \]

\[ R_p = \frac{R_1}{R_2} // R_3 \]

FIGURE 19. MF10 Offset Voltage Sources

For most applications, the outputs are AC coupled and DC offsets are not bothersome unless large signals are applied to the filter input. However, larger offset voltages will cause clipping to occur at lower AC signal levels, and clipping at...
3.0 Applications Information

(Continued)

any of the outputs will cause gain nonlinearities and will change $f_O$ and $Q$. When operating in Mode 3, offsets can become excessively large if $R2$ and $R4$ are used to make $f_{CLK}/f_O$ significantly higher than the nominal value, especially if $Q$ is also high. An extreme example is a bandpass filter having unity gain, a $Q$ of 20, and $f_{CLK}/f_O = 250$ with pin 12 tied to ground (100:1 nominal). $R4/R2$ will therefore be equal to 6.25 and the offset voltage at the lowpass output will be about $+1V$. Where necessary, the offset voltage can be adjusted by using the circuit of Figure 20. This allows adjustment of $V_{OS1}$, which will have varying effects on the different outputs as described in the above equations. Some outputs cannot be adjusted this way in some modes, however ($V_{OS(BP)}$ in modes 1a and 3, for example).

3.5 SAMPLED DATA SYSTEM CONSIDERATIONS

The MF10 is a sampled data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The MF10’s sampling frequency is the same as its clock frequency.) If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled data system, it will be “reflected” to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_c/2 + 100$ Hz will cause the system to respond as though the input frequency was $f_c/2 - 100$ Hz. This phenomenon is known as “aliasing”, and can be reduced or eliminated by limiting the input signal spectrum to less than $f_c/2$. This may in some cases require the use of a bandwidth-limiting filter ahead of the MF10 to limit the input spectrum. However, since the clock frequency is much higher than the center frequency, this will often not be necessary.

Another characteristic of sampled-data circuits is that the output signal changes amplitude once every sampling period, resulting in “steps” in the output voltage which occur at the clock rate (Figure 21). If necessary, these can be “smoothed” with a simple R–C low-pass filter at the MF10 output.

The ratio of $f_{CLK}$ to $f_c$ (normally either 50:1 or 100:1) will also affect performance. A ratio of 100:1 will reduce any aliasing problems and is usually recommended for wideband input signals. In noise sensitive applications, however, a ratio of 50:1 may be better as it will result in 3 dB lower output noise. The 50:1 ratio also results in lower DC offset voltages, as discussed in Section 3.4.

The accuracy of the $f_{CLK}/f_O$ ratio is dependent on the value of $Q$. This is illustrated in the curves under the heading “Typical Performance Characteristics”. As $Q$ is changed, the true value of the ratio changes as well. Unless the $Q$ is low, the error in $f_{CLK}/f_O$ will be small. If the error is too large for a specific application, use a mode that allows adjustment of the ratio with external resistors.

It should also be noted that the product of $Q$ and $f_c$ should be limited to 300 kHz when $f_O < 5$ kHz, and to 200 kHz for $f_O > 5$ kHz.

FIGURE 21. The Sampled-Data Output Waveform
3.0 Applications Information (Continued)

Connection Diagram

Surface Mount and Dual-In-Line Package

Top View

Order Number MF10CCWM
See NS Package Number M20B
Order Number MF10ACN or MF10CCN
See NS Package Number N20A

www.national.com 26
Physical Dimensions  inches (millimeters)
unless otherwise noted

Molded Package (Small Outline) (M)
Order Number MF10ACWM or MF10CCWM
NS Package Number M20B

20-Lead Molded Dual-In-Line Package (N)
Order Number MF10ACN or MF10CCN
NS Package Number N20A
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